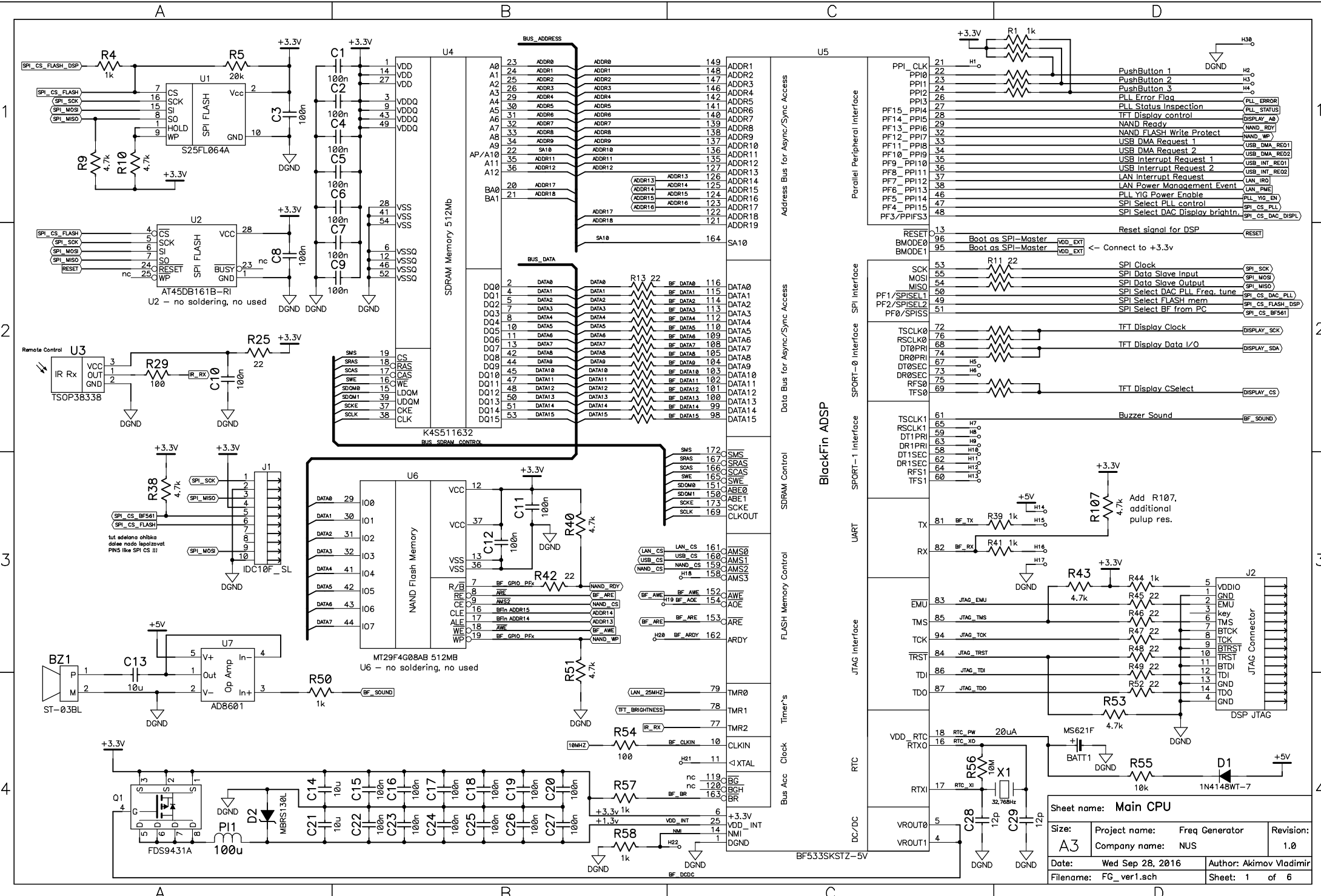


PCB connector here						
RES1	CS	+3.3v	SDA	RES	LEDA	DGND
RES2	DGND	+3.3v	SCK	A0	DGND	LEDK

2 pins do not used

Title			Front panel, buttons & display		
Size	Number		Rev		4
A4					
Date			Drawn by		
Filename			Sheet		of

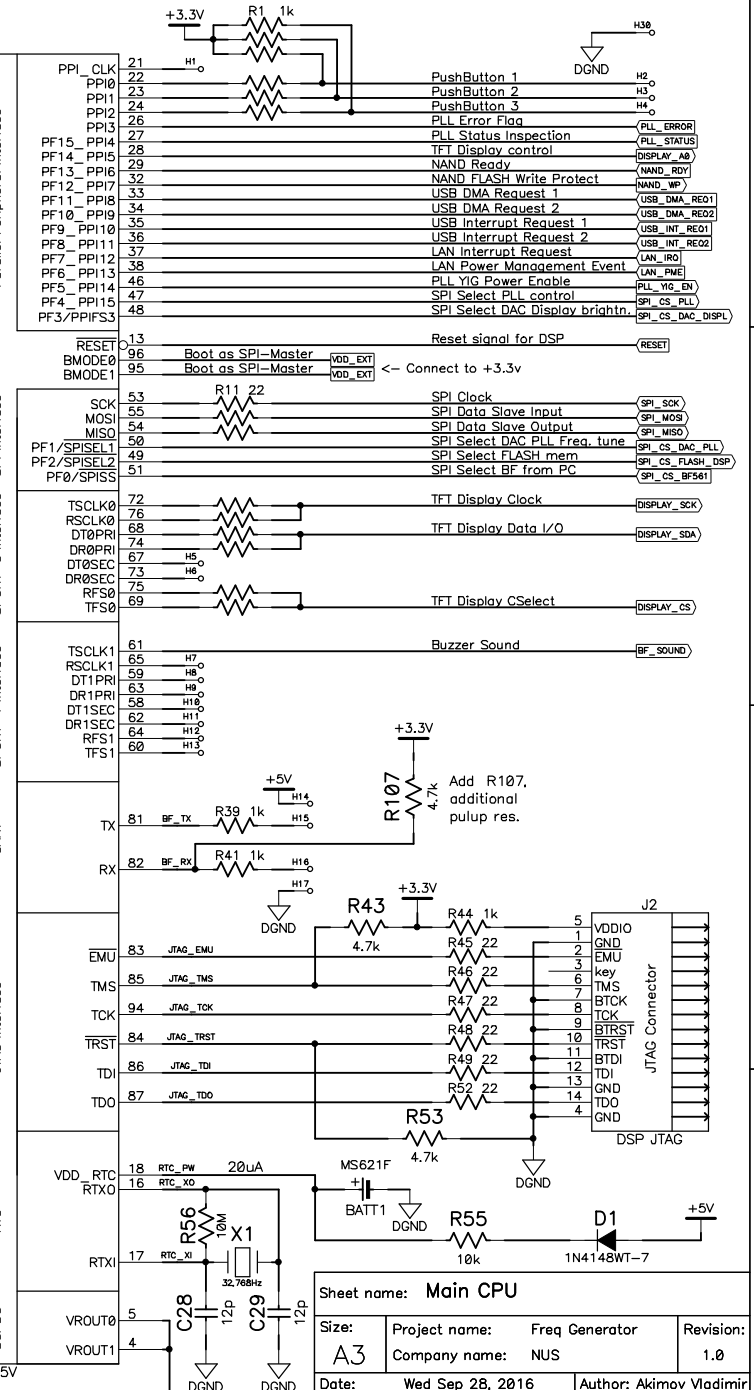
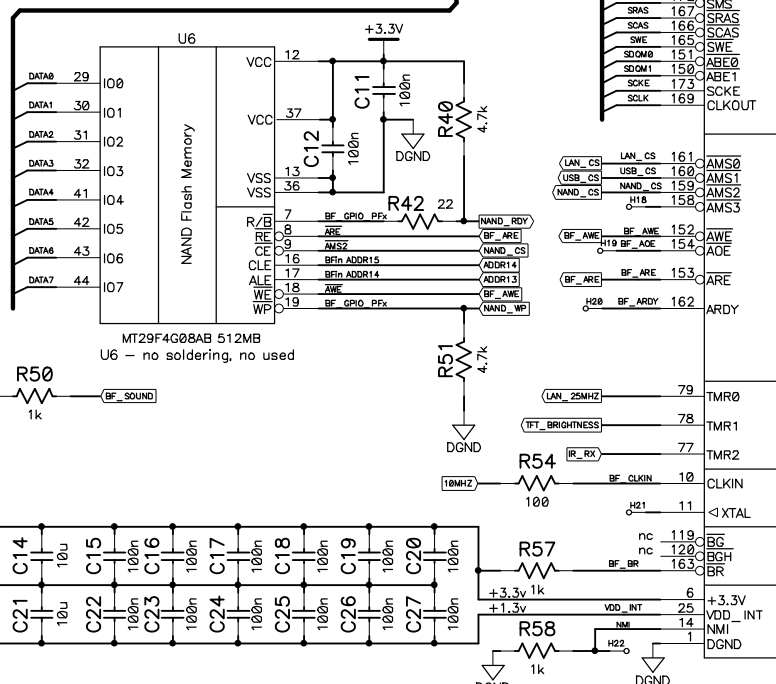


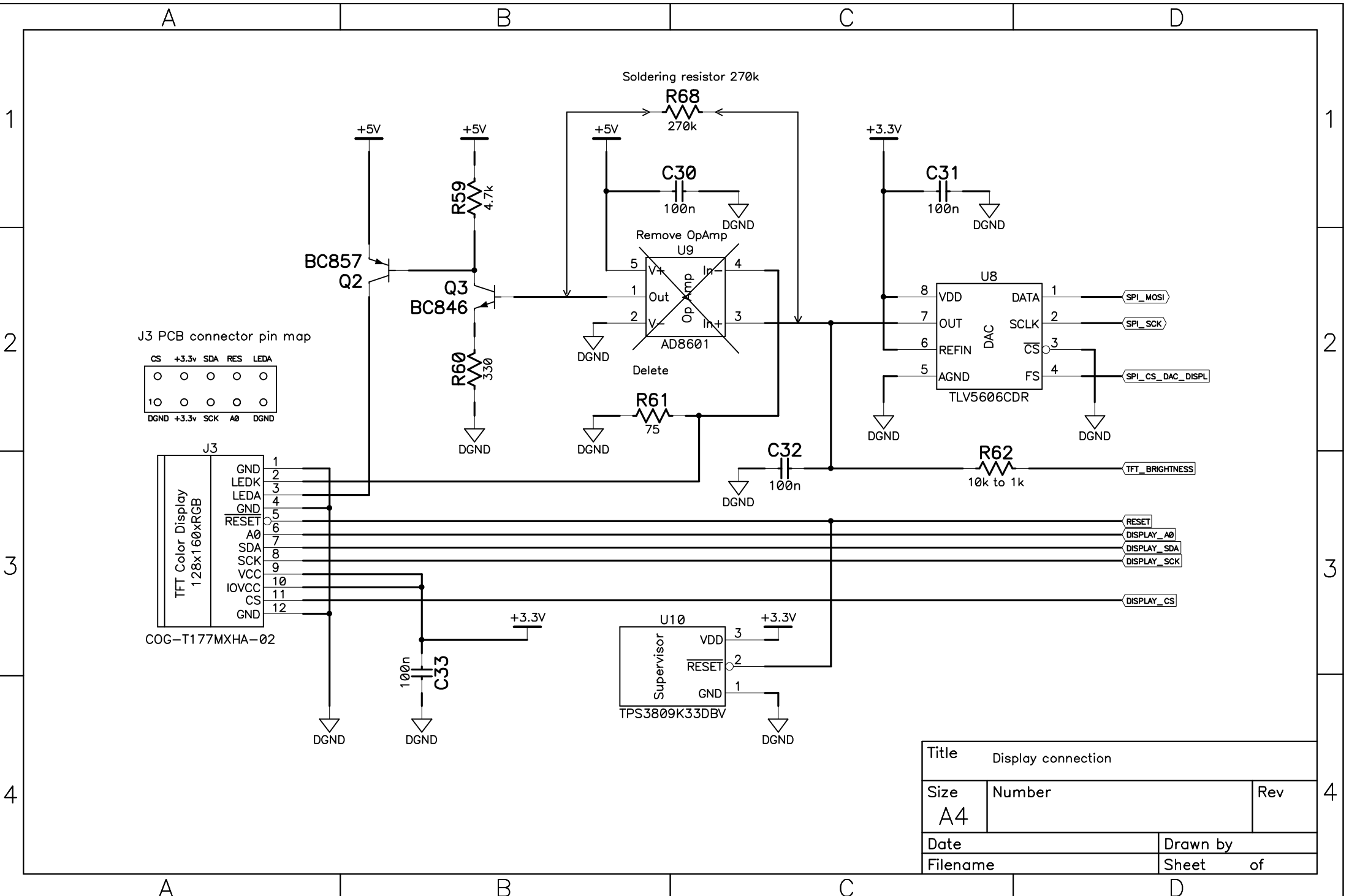
Sheet name: Main CPU

Size: A3	Project name: Freq Generator	Revision: 1.0
Date: Wed Sep 28, 2016	Company name: NUS	Author: Akimov Vladimir
Filename: FG_ver1.sch	Sheet: 1 of 6	

BlackFin ADSP

Address Bus for Async/Sync Access
 Data Bus for Async/Sync Access
 SPORT-0 Interface
 SPORT-1 Interface
 UART
 JTAG Interface
 Timer's
 Bus Acc Clock
 DC/DC





J3 PCB connector pin map

CS	+3.3v	SDA	RES	LEDA
○	○	○	○	○
10	○	○	○	○
DGND	+3.3v	SCK	A0	DGND

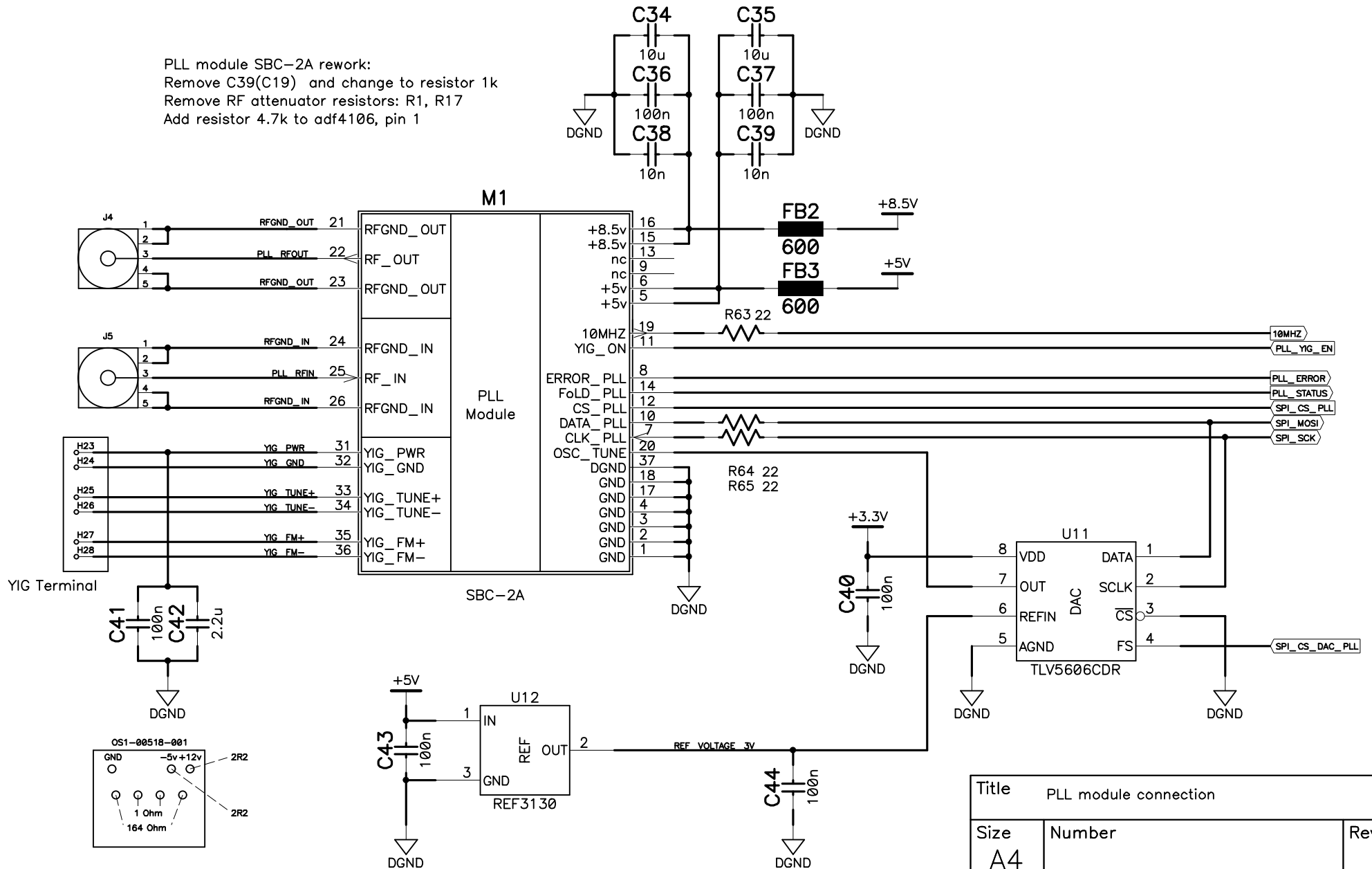
J3

GND	1
LEDK	2
LEDA	3
GND	4
RESET	5
A0	6
SDA	7
SCK	8
VCC	9
IOVCC	10
CS	11
GND	12

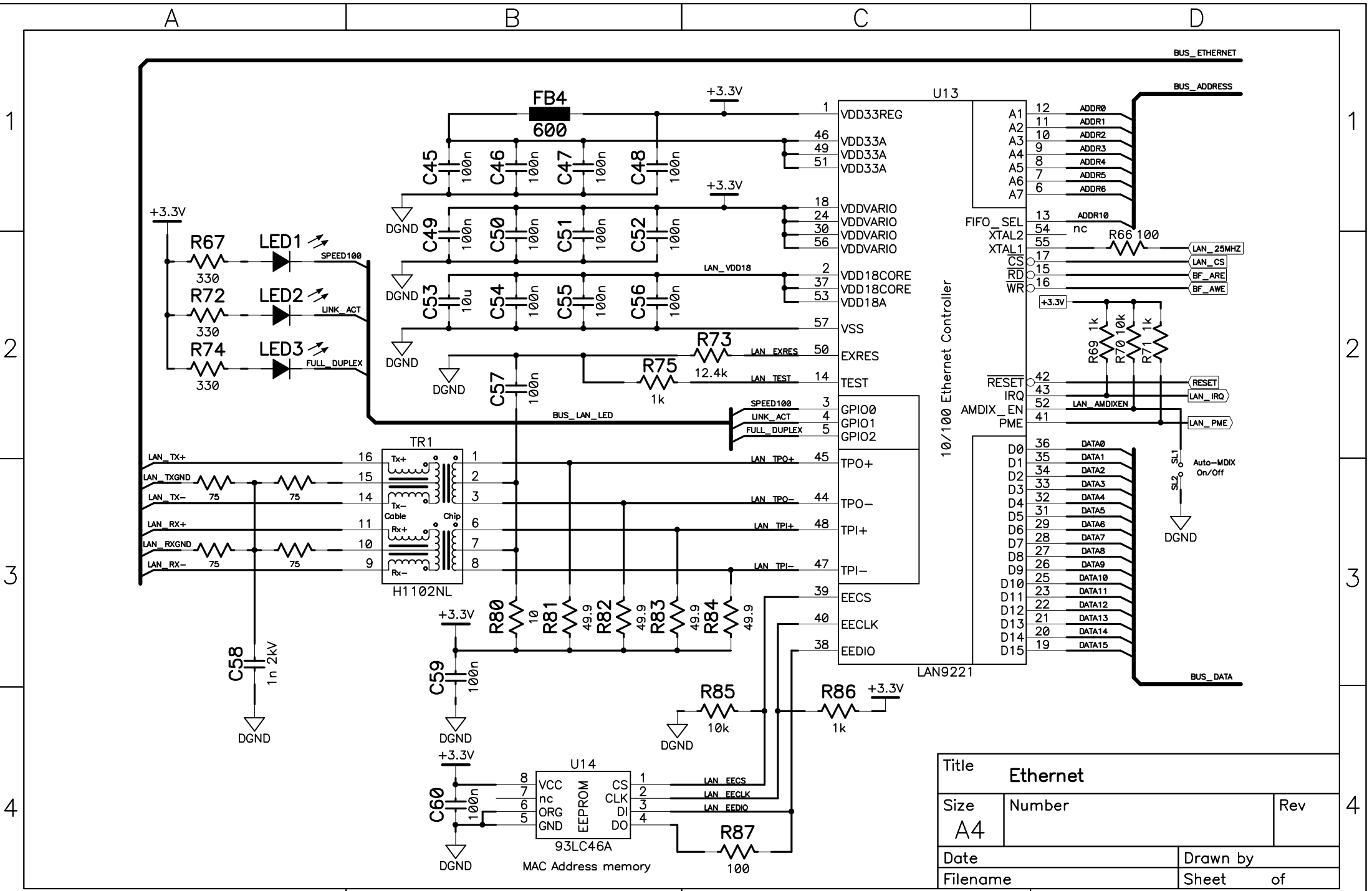
TFT Color Display
128x160xRGB
COG-T177MXHA-02

Title		Display connection	
Size	Number	Rev	
A4			
Date	Drawn by		
Filename	Sheet	of	

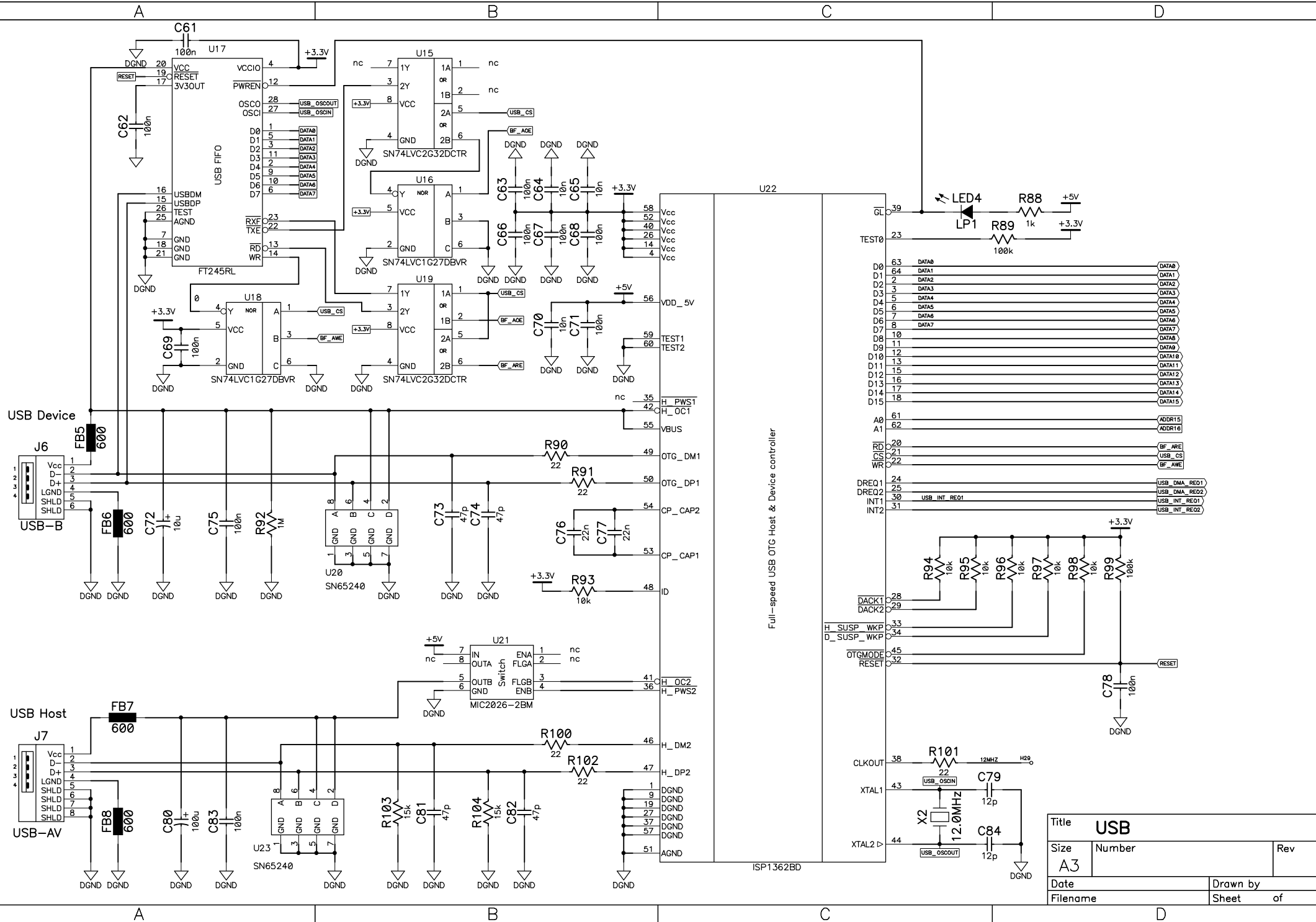
PLL module SBC-2A rework:
 Remove C39(C19) and change to resistor 1k
 Remove RF attenuator resistors: R1, R17
 Add resistor 4.7k to adf4106, pin 1



Title			PLL module connection		
Size	Number		Rev		
A4					
Date			Drawn by		
Filename			Sheet		of



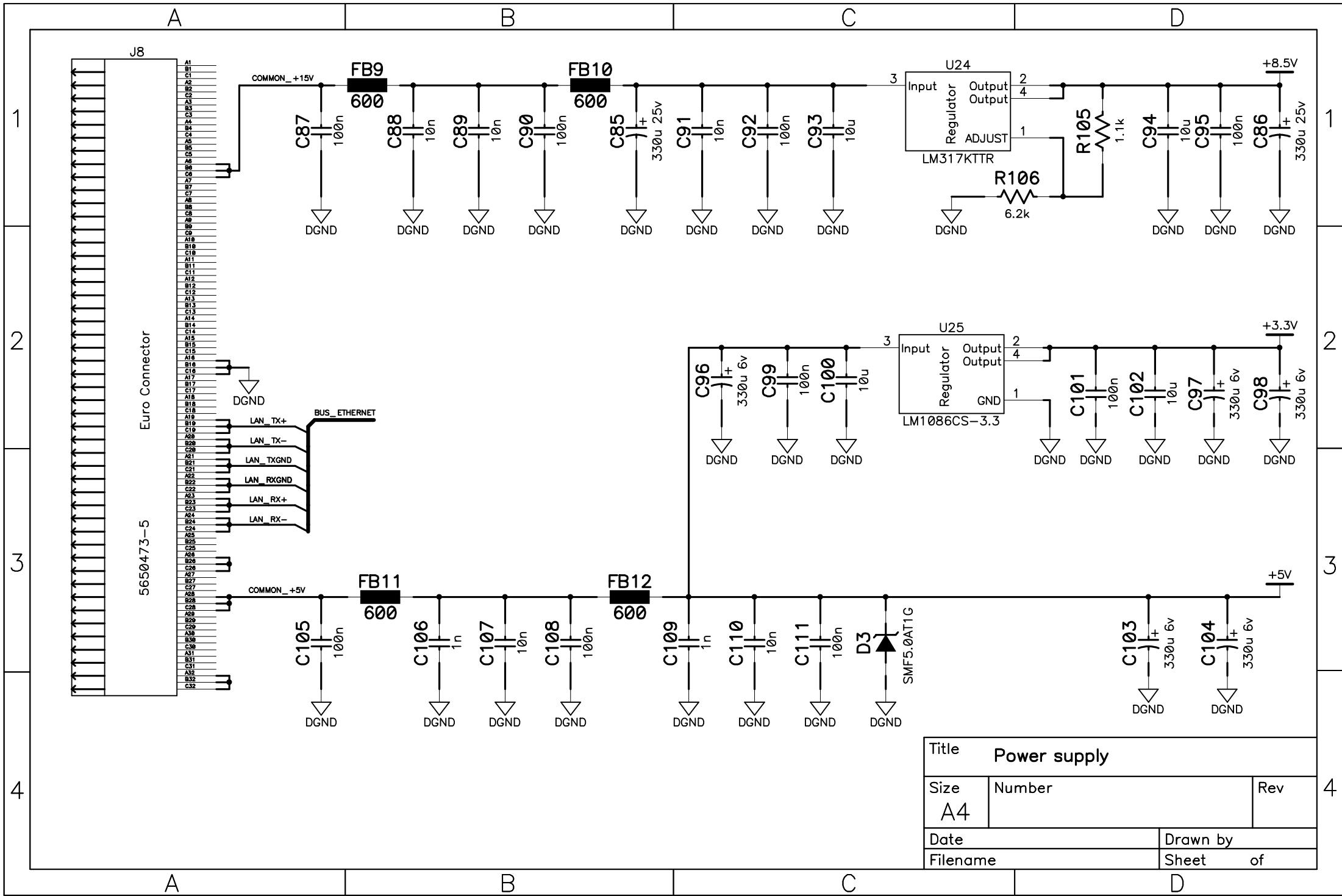
Title			Ethernet		
Size	Number		Rev		
A4					
Date			Drawn by		
Filename			Sheet of		



Full-speed USB OTG Host & Device controller

ISP1362BD

Title USB		
Size A3	Number	Rev
Date	Drawn by	
Filename	Sheet of	



Title			Power supply		
Size	Number				Rev
A4					
Date			Drawn by		
Filename			Sheet	of	